Resistive Bridge Fault Simulation and Analysis for Resistive RAM

N. Arshad, N.Z. Haron, F. Salehuddin
CeTRI, Faculty of Electronic and Computer Engineering
Universiti Teknikal Malaysia Melaka, Hang Tuah Jaya
76100, Durian Tunggal, Melaka, Malaysia
m021220001@student.utem.edu.my,
{zaidi,fauziyah}@utem.edu.my

N. Soin
Department of Electrical Engineering
University of Malaya
50603, Kuala Lumpur, Malaysia
norhayatisoin@um.edu.my

***Abstract*— Resistive Random-Access Memory (ReRAM) is an interesting emerging memory technology to replace conventional memory devices. ReRAM offers many attractive advantages like densest data storage, non-volatility, fast data access and scalable. Although potentially becoming the main emerging memory, ReRAM still prone to have a defect and fault. Nevertheless, because ReRAM uses a non-CMOS device as its memory cells, any defect might behave differently than the ones happen in the existing semiconductor memories. It means that the available memory tests might not detect defective ReRAM cells, leading to a low quality of manufactured ReRAM products. This paper presents the study of how the ReRAM cells behave when they are impacted by bridge defects. Such a defective behavior is required to develop the efficient memory test. A SPICE simulation was carried out using the Silvaco EDA tools. The simulation shows that bridge defects causes the impacted ReRAM cells to change the stored bit at defect values much lower than the value occur in existing semiconductor memories. This analysis confirms that a new memory test is desired.**

Keywords*— *Bridge defects; memory test; memristor; Resistive Random Access Memory (ReRAM)

I. INTRODUCTION

Resistive Random-Access Memory (ReRAM) is interesting emerging memory technologies that possess the characteristics of all three main existing semiconductor memories. It is anticipated to operate fast as Static RAM (SRAM) due to its nanoscale size. It can be packaged denser than Dynamic RAM (DRAM) because the cells are formed by two-terminal device. The function of this two-terminal device is like Flash memories because the memory cells can retain the stored data even when no power is supplied [1,2]. As reported in [3], the tiny size and non-volatility enable a low-power consumption. Moreover, the simple structure enables ReRAM cell array to be stacked in multiple layers increasing the storage capacity. All these advantages support the Moore's Law prediction in the domain of beyond Complementary Metal Oxide Semiconductor (CMOS).

Even though more and more researchers have put their effort studying this fascinating memory technology, there are many uncovered matters need to be resolved. For instance, research on ReRAM has been focused on its architecture, modeling and fabrication [1,2,3]. However, very little work studies on ensuring the outgoing ReRAM product is free from quality problems, i.e., the manufacturing tests are able to screen out defective components forming the memory devices. The work presented in [4,5,6] has revealed that ReRAM might be impacted by open defects. The authors also introduced innovative memory tests to capture the defects as existing memory tests cannot fulfil the aim. This quality issue is also exacerbated by the manufacturing process variation [7]. A similar issue is also expected to be faced when other defects such as bridges and shorts. More detailed on this defect type can be obtained by referring to [5].

This paper presents the study of how the ReRAM cells behave when they are impacted by bridge defects. Such a defect behavior is required to develop the efficient memory test. A SPICE simulation of bridge defects in the ReRAM cells was carried out using the Silvaco EDA tools. The simulation shows that the bridge defects causes the impacted ReRAM cells to change the stored value at defect values lower than the value occur in existing semiconductor memories. This analysis confirms that a new memory test is desired, which is in our progress.

The rest of the paper is organized as follows. Section II reviews the ReRAM background, including the structure, memristor model, operations and possible bridge defects. Section III presents the results of the defect-free simulation, as well as the bridge defect simulation and analysis. Section IV concludes the paper.

II. RERAM BACKGROUND

This section briefly reviews the ReRAM architecture followed by a ReRAM cell model based on a non-CMOS device known as memristor. Then, the ReRAM read and write operations will be explained. Finally, the possible bridge defects in ReRAM cell array.

A. ReRAM Architecture

Fig. 1 illustrates the ReRAM architecture that comprises four main blocks: the memory cell array, row/column decoder, sense amplifier and read/write selector [4]. Each of the peripheral circuits (row/column decoder, sense amplifier and read/write selector) was designed using 22nm CMOS transistors. Meanwhile, the memory cells are formed using a non-CMOS device known as memristor. In our ReRAM

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model, each memristor is located at each crosspoint of nanobitline (NBL) and nanowordline (NWL) [4,5].

The row/column decoder is used to enable the selected signals connected to the selected NBL and NWL in the memory array. The task to generate write and read signal is taken over by the pulse generator. Sense amplifier (SA) is among the important element in a memory device. SA is assigned to sense the read current of the accessed memory cell. The current will then be converted into a voltage and then be amplified before sending the output data to the data register [9].

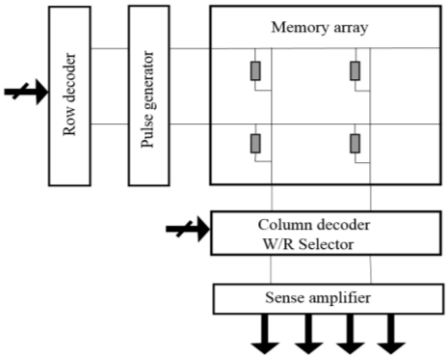


Fig. 1. Functional model of ReRAM [4,5]

B. Memristor Model

Memristor is regarded as the fourth fundamental passive element after the resistor, capacitor and inductor [10]. Unlike the resistor, this non-linear two terminal device can retain the last resistive state it holds when the power is switched off. Obviously, memristor is suitable to be used as nonvolatile memory cells. In 2008, Hewlett-Packard researchers succeeded to come out with a memristor prototype fabricated using two metal electrodes, *Pt* separated by a thin film of titanium oxide (TiO_2) [12]. The thin film with L long is divided into two regions, which are doped (TiO_{2-x}) region with length w and undoped region (TiO_2) with length (L-w) as illustrated in Fig. 2(a). The oxygen vacancies will drift toward the undoped region when a positive voltage is applied until reaches $M=R_{off}$. At this point, the memristor is dominated by doped carriers and is considered as logic 1. On the other hand, the oxygen vacancies drift toward the doped region until it reaches $M=R_{on}$ when a negative voltage is applied. The oxygen vacancies will stop and remain fixed when the power supply is removed.

Recently, many memristor models have been proposed based on its physical and electrical characteristics. The memristor SPICE model proposed by D. Biolek et al. is being implemented in this work [11]. They modified the ideal Strukov's [12] memristor by considering the boundary effect. The model is described as [13]:

$$R(q(t)) = R_{off} + \frac{R_{on} - R_{off}}{ae^{-4kq(t)} + 1}; \mathrm{a} = \frac{R_{ini} - R_{off}}{R_{off} - R_{ini}} \quad (1)$$

Where R_{on} and R_{off} are limiting values of memristance and k is a constant. Equation (1) represents the memristance as a function of the native state variable q. Fig. 2 (c) shows the hysteresis loop of the memristor.

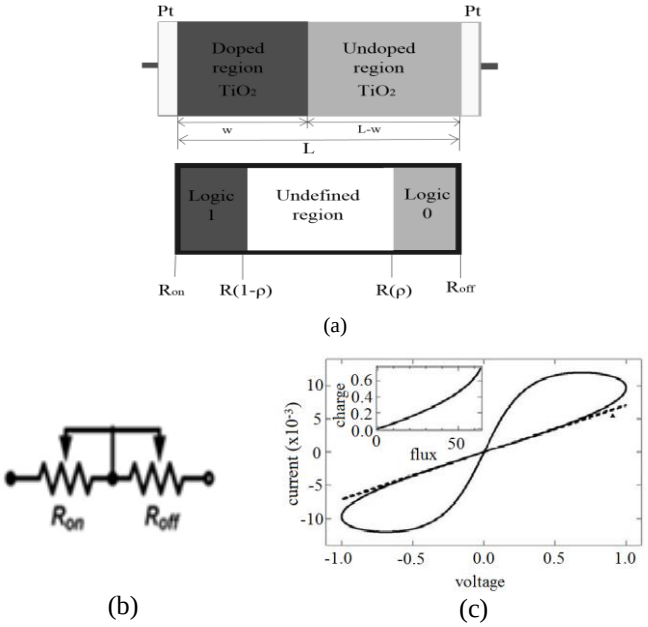


Fig. 2. Memristor: (a) model (b) electrical equivalent circuit (c) I-V curve

C. ReRAM Operation

There are two operations that can be performed by ReRAM: write and read operations. Write operation can be accomplished by applying the appropriate voltage polarity and time duration [4,5]. Applying -1V at a certain time duration to one of the memristor terminals while grounding the other terminal will set the memristance from $M=R_{off}$ to $M=R_{on}$; when the supply is changed to 1V at a certain time duration, the memristance changes from $M=R_{on}$ to $M=R_{off}$. This operation is illustrated in Fig. 3.

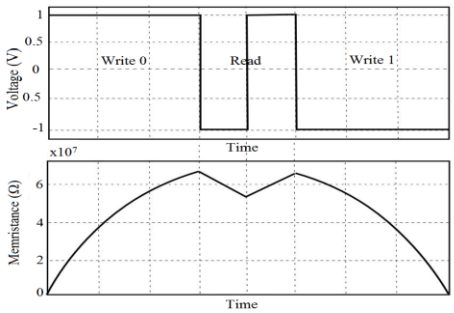
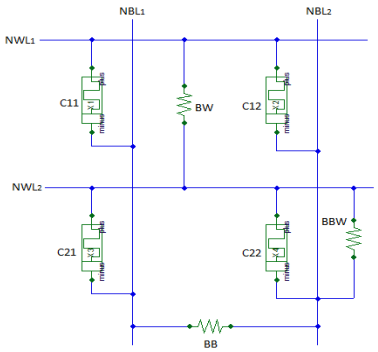


Fig. 3. Changes in memristance due to voltage versus time [6]

Two phases of read operation are needed to ensure that the memristor retain its memristance after the read operation [4,5]. A zero net change in memristance is important during read operation, so a negative pulse is supplied followed immediately with positive pulse with the same magnitude and duration. The bottom part of Fig. 3 depicts the behavior of a memristor during the read operation.

D. Bridge Defect in ReRAM

Bridge defects are one of the defect types commonly occurred in the memory cell array [5]. Fig. 4 illustrates the possible bridge defect that can occur in the ReRAM cell array. These defect types might occur due to an unintended longer nanowire connected to its adjacent nanowire. For instance, a bridge defect between NBL_1 and NBL_2 (BB) can flip the data stored in cell C_{22} when operation of read is performed to C_{21}.



Legend:	
BB	Bridge between NBLs
BW	Bridge between NWLs
BBW	Bridge between NBLs and NWLs

Fig. 4. Possible bridge defects in the memory cell array

III. SIMULATION AND ANALYSIS

This section presents the result of the simulation and analysis of bridge defects in the ReRAM cell array. The section starts with the simulation results for defect-free and bridge-defective ReRAM. It is followed by the analysis of bridge defect simulation whereby the discrepancy between the ReRAM cells behavior under the defect-free and bridge defect cases is studied.

A. Defect-free Simulation Setup and Results

Before continuing with bridge defect injection, a defect-free ReRAM SPICE model was designed and simulated using the Silvaco EDA simulation tools. As 22nm CMOS technology was used to design the ReRAM components other than the memory cell array, so the supply voltage (V_{DD}) that used is 0.95V [14]. The CMOS logic levels for this technology node are illustrated in Fig. 5. $V_{H(max)}$ = 0.95V is the maximum high voltage value and $V_{H(min)}$ = 0.63V is the minimum high-voltage value. Logic 0 is presented by maximum low voltage $V_{L(max)}$ = 0.32V and minimum low voltage $V_{L(min)}$ = 0V. The voltage value between $V_{H(min)}$ and $V_{L(max)}$ is in an undefined state.

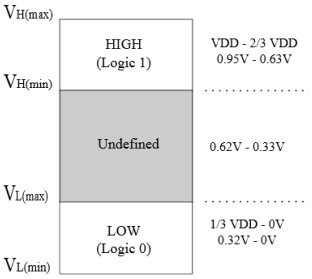


Fig. 5. 22nm CMOS logic levels

Fig. 6 shows the simulation result for the sequence *S0 = w0(C_{11}), r0(C_{11}), w1(C_{21}), r1(C_{21}).* The sequence is to write logic 0 to C_{11} and then read it with the expectation that logic 0 will be retrieved. Next, logic 1 is written to C_{21} and then read it with the expectation that logic 1 will be retrieved. During the operation, several control signals are involved as shown in Fig. 6: (i) write and read signal; v(w/r), (ii) sense signal, which is on during half cycle of read operation; v(sense) and (iii) output voltage; v(out1). The v(out1) is measured at the output of the sense amplifier. It represents the voltage of the read ReRAM cell. When C_{11} is read, the sense amplifier will give the value of 0V meaning that the cell stores the correct logic 0 values. The same goes to C_{12} whereby when reading it gives the output voltage 0.88V that is translated as logic 1 state. C_{11}

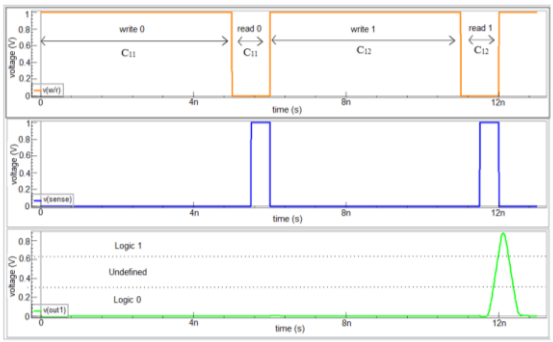
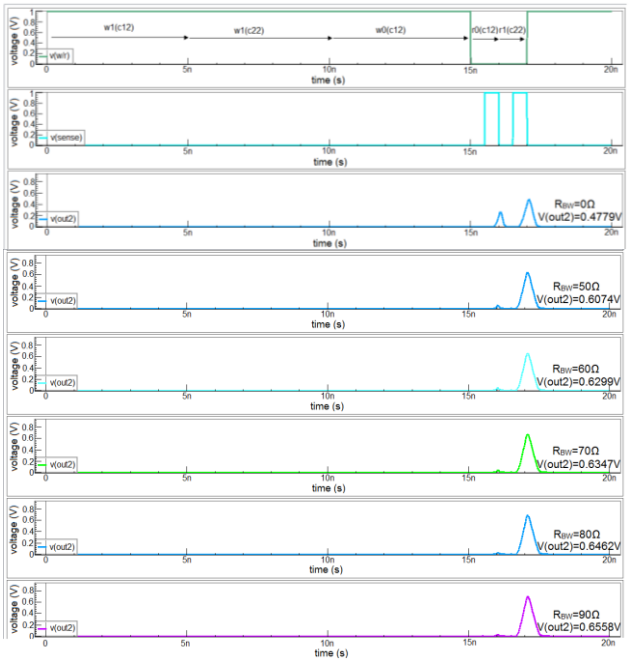


Fig. 6. Defect-free simulation result

B. Bridge Defect Simulation Setup and Results

For this simulation, bridge defects are modeled electrically using the resistor between two NBLs, between two NWLs, and between one NBL and one NWL, as shown in Fig. 4. For each bridge location, the resistor values are swept between $0\Omega \leq R_{bridge} \leq 1000\Omega$. Due to space limitation, only the simulation result for BW is illustrated in the graph as shown in Fig. 7. The simulation results for BB and BBW is given in Table III and Table V.



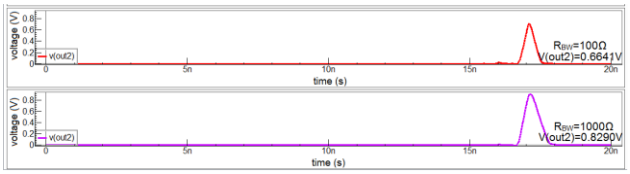


Fig. 7. Bridge defect simulation results

Fig. 7 shows the simulation results of BW for the sequence *S1 = w1(C_{12}),w1(C_{22}),w0(C_{12}),r0(C_{12}),r1(C_{22})* with different value of R_{BW}. In this sequence, C_{12} is the aggressor cell while C_{22} is the victim cell. The simulation shows that at $R_{BW} \leq 60\Omega$, C_{22} that initially is set to logic 1 holds an undefined value when C_{12} is changing state from logic 1 to logic 0. This is because the bridge with low resistive value causes some current (resulting from negative polarity voltage) to overtake through the victim, ReRAM cell (C_{22}) and increases the internal state (memristance) to an undefined value. When the victim cell is read, the sense amplifier might produce incorrect logic state. However, as the resistor values $R_{BW} > 60\Omega$, the victim cell is not affected by the bridge.

C. Bridge Defect Simulation Analysis

Table I summarizes the observed faults at different bridge defect values of BW. It shows that the victim's cell (C_{22}) starts to be affected by the defect when $0\Omega \leq R_{BW} \leq 59\Omega$. At this bridge defect range, the cell will start to drop to the undefined level from its initial state, which is logic 1. Undefined level will cause a random logic value to be read from the defective ReRAM cells [4]. Meanwhile, the aggressor cell (C_{12}) remains in its state, which is logic 0 (low). Table II illustrate the summary of logic level for this bridge defect, BW.

Table III presents the summary of faults results for bridge defect type BB. The sequence used in this simulation was *S2 = w1(C_{11}), w1(C_{12}), w0(C_{11}), r0(C_{11}), r1(C_{12}).* The table shows that the logic level of the victim cell drops to low (logic 0) when $0\Omega \leq R_{BB} \leq 35\Omega$. Meanwhile, the victim cell might give the undefined value during read operation when $36\Omega \leq R_{BB} \leq 370\Omega$. However, the victim cell remains in its expected value if $373\Omega \leq R_{BB} \leq 1000\Omega$. The logic level for this bridge defect, BB is summarized in Table IV.

However, faults due to BBW give different results as shown in Table V. The victim cell that involved with this defect is C_{12} since the resistive bridge defect occurs between NBL_2 and NWL_2. The same sequence was applied; i.e., *S1 = w1(C_{12}),w1(C_{22}),w0(C_{12}),r0(C_{12}),r1(C_{22}).* Table V shows the output voltage at the second row of sense amplifier and Table VI illustrates the summary for the logic level. The output voltage is low when the bridge is between 220Ω till 1000Ω.

Unfortunately, the output voltage shows fault value when the bridge is between 0Ω to 210Ω. The cell gives logic 1 when $0\Omega \leq R_{BBW} \leq 130\Omega$ and undefined value if $139\Omega \leq R_{BBW} \leq 210\Omega$. BBW defect affect C_{12} because the resistor act as internal resistance to the victim cell. However, the adjacent cell (C_{22}) also affected when the resistive bridge values too low (0Ω - 30Ω).

TABLE I. OBSERVED FAULTS FOR BW

Bridge (Ω)	Output voltage at accessed cells (V)			
	Aggressor cell (C_{12})	*Logic level (C_{12})*	*Victim cell (C_{22})*	*Logic level (C_{22})*
0	0.2619	Low	0.4779	Undefined
10	0.1864	Low	0.5236	Undefined
20	0.1315	Low	0.5577	Undefined
30	0.0916	Low	0.5858	Undefined
40	0.0635	Low	0.6089	Undefined
50	0.0452	Low	0.6074	Undefined
60	0.0345	Low	0.6299	High
70	0.0270	Low	0.6347	High
80	0.0224	Low	0.6462	High
90	0.0193	Low	0.6558	High
100	0.0169	Low	0.6641	High
1000	0.0048	Low	0.8290	High

TABLE II. SUMMARY OF LOGIC LEVEL FOR BW

Logic level	Range of resistive bridge defect (Ω)	
	Aggressor cell (C_{12})	*Victim cell (C_{22})*
High	Remain its initial state for read 0 operations	$60 \leq R_{BW} \leq 1000$
Undefined		$0 \leq R_{BW} \leq 59$
Low		-

TABLE III. OBSERVED FAULTS FOR BB

Bridge (Ω)	Output voltage at accessed cells (V)			
	Aggressor cell (C_{11})	*Logic level (C_{11})*	*Victim cell (C_{12})*	*Logic level (C_{12})*
0	0.0819	Low	0.1417	Low
10	0.0517	Low	0.2057	Low
20	0.0362	Low	0.2593	Low
30	0.0283	Low	0.3042	Low
35	0.0241	Low	0.3239	Low
36	0.0228	Low	0.3273	Undefined
40	0.0223	Low	0.3417	Undefined
50	0.0183	Low	0.3718	Undefined
60	0.0167	Low	0.3959	Undefined
70	0.0147	Low	0.4222	Undefined
80	0.0135	Low	0.4434	Undefined
90	0.0125	Low	0.4607	Undefined
100	0.0117	Low	0.4759	Undefined
200	0.0083	Low	0.5634	Undefined
300	0.0072	Low	0.6020	Undefined
350	0.0069	Low	0.6141	Undefined
360	0.0068	Low	0.6162	Undefined
370	0.0068	Low	0.6182	Undefined
372	0.0067	Low	0.6344	Undefined
380	0.0065	Low	0.8395	High
390	0.0064	Low	0.8411	High
400	0.0064	Low	0.8426	High
1000	0.0052	Low	0.8763	High

TABLE IV. SUMMARY OF LOGIC LEVEL FOR BB

Logic level	Range of resistive bridge defect (Ω)	
	Aggressor cell (C_{12})	*Victim cell (C_{22})*
High	Remain its initial state for read 0 operations	$373 \leq R_{BB} \leq 1000$
Undefined		$36 \leq R_{BB} \leq 372$
Low		$0 \leq R_{BB} \leq 35$

TABLE V. OBSERVED FAULTS FOR BBW

Bridge (Ω)	Output voltage at accessed cells (V)			
	Victim cell (C_{12})	*Logic level (C_{12})*	*Adjacent cell (C_{22})*	*Logic level (C_{22})*
0	0.9630	High	0.2444	Low
10	0.9629	High	0.2668	Low
20	0.9625	High	0.2828	Low
30	0.9590	High	0.7753	High
40	0.9543	High	0.8059	High
50	0.9463	High	0.8214	High
60	0.9339	High	0.8219	High
70	0.9157	High	0.8103	High
80	0.8903	High	0.7982	High
90	0.8573	High	0.7892	High
100	0.8170	High	0.7820	High
110	0.7716	High	0.7763	High
120	0.7237	High	0.7721	High
130	0.6758	High	0.7689	High
140	0.6110	Undefined	0.8154	High
150	0.5654	Undefined	0.8167	High
160	0.5225	Undefined	0.8183	High
170	0.4823	Undefined	0.8201	High
180	0.4485	Undefined	0.8222	High
190	0.4100	Undefined	0.8244	High
200	0.3778	Undefined	0.8266	High
210	0.3479	Undefined	0.8288	High
220	0.3203	Low	0.8311	High
230	0.2949	Low	0.8332	High
240	0.2714	Low	0.8354	High
250	0.2499	Low	0.8375	High
260	0.2298	Low	0.8395	High
270	0.2114	Low	0.8415	High
280	0.1944	Low	0.8434	High
290	0.1788	Low	0.8453	High
300	0.1644	Low	0.8471	High
400	0.0694	Low	0.8616	High
500	0.0333	Low	0.8714	High
1000	0.0101	Low	0.8919	High

TABLE VI. SUMMARY OF LOGIC LEVEL FOR BBW

Logic level	Range of resistive bridge defect (Ω)	
	Victim cell (C_{12})	*Adjacent cell (C_{22})*
High	$0 \leq R_{BBW} \leq 130$	Remain its initial state for read 1 operations
Undefined	$139 \leq R_{BBW} \leq 210$	
Low	$220 \leq R_{BB} \leq 1000$	$0 \leq R_{BBW} \leq 30$

IV. CONCLUSION

This paper presented a bridge defect simulation and analysis for ReRAM cell array. Firstly, a defect-free ReRAM model was designed and simulated in order to ensure that the simulation provide the correct results. Next, the resistors that represent bridge defects are added to the defect-free model. Then, simulations were carried out and the behaviors of the ReRAM cells were observed and analyzed. It shows that bridge defects only cause problems when the defect value is small. However, these defects must be detected as existing test algorithms only detect such defects with much higher defect value. For this aim, our future work is to develop a test algorithm based on design-for-testability (DfT) schemes, specifically to detect bridge defects in the ReRAM cell array.

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