Small Signal Modelling of InGaAs/InAlAs pHEMT for low noise applications

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***Abstract*—This paper presents the small signal modelling of high breakdown InP pseudomorphic High Electron Mobility Transistors (pHEMT) that have been developed and fabricated at the University of Manchester [1] for low noise applications mainly for the Square Kilometre Array (SKA) project. The ultra-low leakage properties of a novel InGaAs/InAlAs/InP pHEMTs structure were used to fabricate a series of transistor with total gate width ranging from 0.2 mm to 1.2 mm. The measured DC and S-Parameters data from the fabricated devices were then used for the transistors' modelling. The transistors demonstrated to operate up to frequencies of 25 GHz. These transistors models are used in the design of Low Noise Amplifiers (LNAs) using fully Monolithic Microwave Integrated Circuit (MMIC) technology**

Keywords— InGaAs/InAlAs; InP; pHEMT; Square Kilometre Array (SKA); LNA; MMIC

I. INTRODUCTION

Nowadays, great progress has been made in the design and manufacture of InP based pHEMT devices particularly in low noise applications. This technology together with advances in MMIC technology, is driving future high volume, low cost, high performance millimetre-wave applications with high prospects [1]. The vital parameter for low noise that is cut-off frequencies (f_T) have been demonstrated in the THz range with this InP based pHEMT devices [2-4]. The unique and inherent properties of the carriers in a 2-DEG provide the device with high electron mobility and high sheet carrier density, making it the best device selection for many electronic applications. Recently, a novel strained InGaAs-InAlAs pHEMT devices having extremely high breakdown and low noise properties has been reported [5]. These devices show a great promise for use as a low cost high performance LNA for the intermediate frequency band of the SKA.

The MMIC manufacturing is time consuming and costly, since the correct functionality of the circuit can only be checked after the whole fabrication is completed. Therefore, an accurate small signal and large signal model of a device or transistor is an essential requirement for any circuit design either for Complementary Metal Oxide Semiconductor (CMOS) or HEMT technology before commencing the fabrication process. For that reason, there is a continuous effort from circuit designers to produce efficient transistor models since it was first developed by Curtice, 1980 [6]. A decade later, several empirical small signal and large signal models had been developed in order to allow the model being extracted to use Computer Aided Design (CAD) tools [7]. As significance, this research focuses on the characterization and accurate small signal modelling of advance material InP based pHEMT transistors using Advance Design System (ADS) Software.

XMBE144	**VMBE2100**
(Cap) $In_{0.53}Ga_{0.47}As$ *50 Å*	(Cap) $In_{0.53}Ga_{0.47}As$ *50 Å*
(Barrier) $In_{0.52}Al_{0.48}As$ *300 Å*	(Barrier) $In_{0.3}Al_{0.7}As$ *300 Å*
δ-doped	δ-doped
(Spacer) $In_{0.52}Al_{0.48}As$ *100 Å*	(Spacer) $In_{0.3}Al_{0.7}As$ *100 Å*
(Channel) $In_{0.7}Ga_{0.3}As$ *140 Å*	(Channel) $In_{0.7}Ga_{0.3}As$ *160 Å*
(Buffer) $In_{0.52}Al_{0.48}As$ *4500 Å*	(Buffer) $In_{0.52}Al_{0.48}As$ *4500 Å*
(Substrate) InP Fe doped	(Substrate) InP Fe doped

Fig. 1: Two different epitaxial layer structures for device under test

II. TRANSISTOR CHARACTERISTICS

In this work, a number of devices fabricated from two main types of epitaxial layer have been modelled for the use in low noise applications. The two different epitaxial layers are denoted as XMBE144 and VMBE2100. The effective gate length for all devices used in this study is 1 µm while gate widths of the devices are ranging from 0.2 mm to 1.2 mm. All epitaxial layers were grown using The University of Manchester Molecular Beam Epitaxy (MBE) on RIBER V100H and V90H systems. These epitaxial layers were grown to improve the overall performance of the LNA through optimisation of the devices' epitaxial layers. Performance enhancement of XMBE144 and VMBE2100 was achieved through epitaxial layer improvements, resulting in low gate leakage and an enhancement in the devices' thermal stability. The epitaxial structures are shown in Fig. 1.

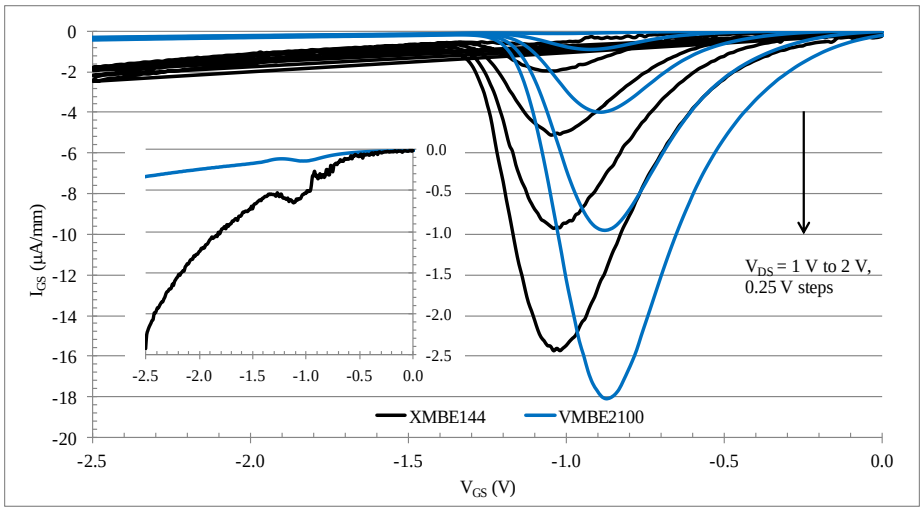


Fig. 2: On-state leakage current for XMBE144 and VMBE2100. Inset is the on-state leakage current of V_{DS} = 1 V (4 x 200 μm devices)

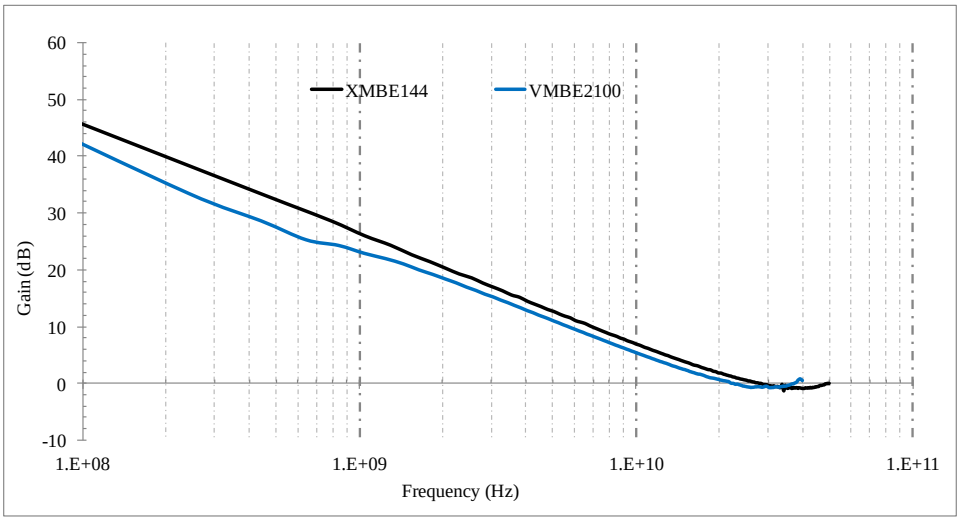


Fig. 3: Unity current gain (h21) plot versus frequency at VDS = 1 V. The f_T is obtained by the 0 dB crossing at x-axis (frequency)

The epitaxial structures of XMBE 144 and VMBE2100 share almost the same epitaxy layers and thicknesses. The only difference between these two materials is the Schottky Barrier layer for VMBE2100 is made from highly strained, high band gap (~2.1 eV) material, which is advantageous for achieving a higher Schottky barrier height, and consequently leads to a lower gate leakage current. Besides, the epilayers are made from δ-doped structures to further enhance the carrier confinement in the quantum well, and additionally reduced the gate leakage. Fig.2 shows the on-state leakage current for XMBE144 and VMBE2100. It is obvious that the VMBE2100 device's leakage current is lower than XMBE144 through the adoption of wider band gap material as the Schottky barrier layer.

The cut-off frequency (f_T) for these epilayers are ~ 25 GHz as depicted in Fig. 3, is among the highest has been reported for 1 μm devices.

This higher f_T performance is fundamental parameter for the devices' low noise characteristics as given by Fukui's minimum noise figure expression:

$$F_{min} = 1 + k_1 \frac{f}{f_T} \sqrt{g_m \left(R_s + R_g \right)} \qquad (1)$$

III. TRANSISTOR SMALL SIGNAL MODELLING

There are two techniques of device modeling; physical and empirical models. Both modeling can be used to represent a real device. The selection of the appropriate model depends on the exact requirements of the particular application since each techniques has its own advantages and limitation. In this project, the empirical technique is used to model the fabricated

InGaAs/InAlAs/InP pHEMTs transistor. The empirical modeling begins with the small signal model followed by large signal model. The small signal modelling phase starts with the extraction of extrinsic and intrinsic parameters from pinched and biased dependent S-parameter measurements, from which the initial small signal model is generated.

This model is then optimized by fitting the modelled and measured S-parameters data. This will consequently reduce the modelling error. Large signal modelling of the devices is then performed; the DC and RF data are extracted, modelled and optimized. After the large signal model has been optimized, the complete model is ready to be used in circuit designs. However, this paper only discusses the small signal model of fabricated transistors, as the large signal model will be reported soon.

IV. Results and Discussions

There are several small signal models circuit topologies described in [9-12]. The small signal model presented in this work, developed by Dambrine *et al.* [10], is the most commonly used. The most widely used equivalent circuit model for pHEMT/HEMT device is in Figure 4. The S-parameter measurements are firstly exported from the ICCAP to the ADS software, where the small signal model is created. The configuration of the transistor's small signal model begins with the extraction of 8 extrinsic parameters, followed by the 7 intrinsic parameters. The extrinsic parameters are obtained from the device's pinched (cold) S-parameters measurement. This measurement is made when the device's channel is totally pinched, and it is bias-independent. Conversely, the intrinsic parameters extraction can be obtained from the bias dependent (hot) measurement. The extraction technique used throughout this project is an analytical method. The small signal model is performed to achieve an excellent fit between the modelled and measured data.

Fig. 5 shows the empirical model with the optimized extrinsic and intrinsic values for the XMBE144 4 x 200 µm device. The S-parameter data is depicted in Figure 6, where the modelled data shows a good fit to the measured data up to a frequency of 10 GHz

TABLE I summarized the extrinsic parameters value while TABLE II summarized the intrinsic parameters value for devices involved in this work.

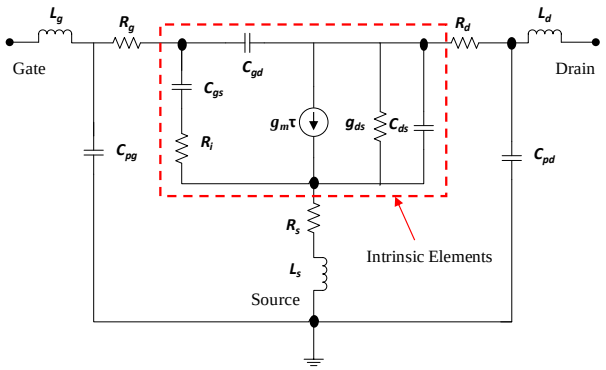


Fig. 4: Standard form of pHEMT/HEMT small signal equivalent circuit [64]

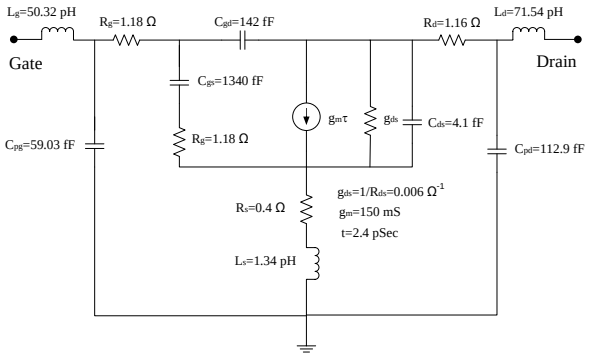
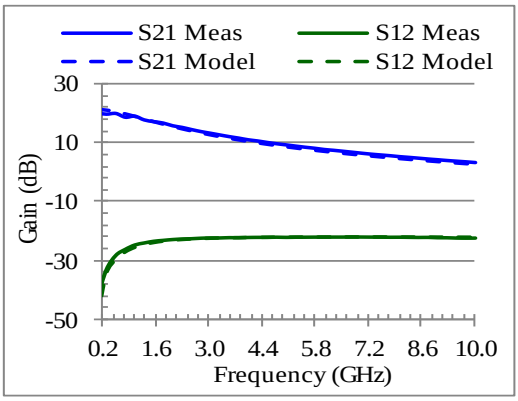
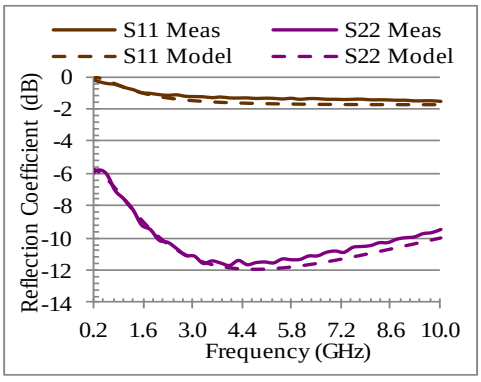


Fig. 5: The optimised Small signal Model (with extrinsic and intrinsic values) for the XMBE144 4 x 200 µm device



(a)



(b)

Fig. 6: The matched S-parameter data after Small signal Model optimisation for XMBE144's 4 x 200 µm device. (a) S21 and S12 and (b) S11 and S22

TABLE I. TABLE OF EXTRINSIC PARAMETERS FOR ALL DEVICES AT V_{DS} = 1 V AND 10% I_{DSS}

Sample ID	Gate fingers x widths (µm)	C_{pg} (fF)	C_{pd} (fF)	R_s (Ω)	R_g (Ω)	R_d (Ω)	L_s (pH)	L_g (pH)	L_d (pH)
XMBE144	2 x 50	7.8	26.6	5.80	1.94	2.91	8.1	20.5	17.9
	2 x 100	13.7	37.9	1.99	1.44	1.38	3.9	26.7	56.1
	4 x 200	59.0	112.9	0.40	1.18	1.16	1.3	50.3	71.5
VMBE2100	4 x 200	40.1	155.6	0.53	1.56	1.43	2.0	79.7	111.6

TABLE II. TABLE OF INSTINSIC PARAMETERS FOR ALL DEVICES AT V_{DS} = 1 V AND 10% I_{DSS}

Sample ID	Gate fingers x widths (µm)	g_m (mS)	τ (psec)	R_i (Ω)	R_{ds} (Ω)	C_{gs} (fF)	C_{ds} (fF)	C_{gd} (fF)
XMBE144	2 x 50	19	1.71	9.42	1318.9	150	1.7	22
	2 x 100	50	1.77	3.89	681.3	410	2.6	43
	4 x 200	150	2.40	1.14	157.9	1340	4.1	142
VMBE2100	4 x 200	170	1.17	2.42	179.0	1400	3.0	150

From the TABLE I, one can see that the capacitance values increase as the total device width is increased. Since the capacitance value is proportional to the contact area, the capacitance increases as the contact pad areas become larger. It can also be seen from TABLE I, that the terminal resistances are also reduced as the device size is increased. As the gate width is increased, the total gate area will increase, and consequently it will decrease the terminal resistances.

The intrinsic parameters follow the same trend as the extrinsic values as the device width is increased. However, a significant reduction in R_{ds} values can be observed as the device width is increased. This resistance can also be viewed as the resistance in the channel between the Drain and Source terminals. As the device width is increased, the total area involved in parallel with the device width will be increased, and consequently the channel resistance is reduced.

V. CONCLUSION

A small signal model for InGaAs/InAlAs/InP pHEMT is successfully presented. The model has been tested for a series of 1 µm InP based transistors [13]. The consistency in obtaining the excellent agreement between modelled and measured data over 10 GHz, verify and validate the analytical technique uses. Having the advantages of an extremely lower gate leakage current and high cut-off frequency, f_T make the

proposed devices one of the primary choices for low noise application, mainly for the SKA satellite [14].

VI. Acknowledgements

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