Design and Analysis of Ultrathin Pillar VDG-MOSFET for Low Power (LP) Technology

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***Abstract*— As transistor's density and dimension have been rapidly shrunk down in every year onwards, it is difficult to design a Metal Oxide Semiconductor Field Effect Transistor (MOSFET) that possesses minimal short channel effect (SCE) problems. One of the most recognized MOSFET architecture which has the ability to circumvent SCE is known as Vertical Double Gate (DG) MOSFET device. The presence of two gates are capable of doubling the channel coupling in Vertical DG-MOSFET device, thus resulting in higher current density. This paper presents a study in which an attempt has been made to virtually design the Ultrathin Pillar (UTP) Vertical Double Gate (VDG) MOSFET device for low power (LP) technology requirements by utilizing SILVACO TCAD tools. Three novel designs which are known as UTP VDG-MOSFET, UTP Silicon-on-insulator (SOI) VDG-MOSFET and UTP Polysilicon-on-insulator (POI) VDG-MOSFET are introduced in order to compare their electrical performance. From the retrieved results, it is observed that UTP POI VDG-MOSFET device is the most suitable design for low power application in which its threshold voltage (V_{TH}) and drive current (I_{ON}) values are correspondingly at 0.419 V and 704.6 µA/µm. These values are observed to be the closest value to the International Technology Roadmap Semiconductor (ITRS) 2013 specification.**

Keywords—ATHENA, ATLAS, POI, SOI, VDG-MOSFET

I. INTRODUCTION

The prediction made by Gordon Moore in 1965 states that the number of transistors per chips would double approximately every two years [1]. When the physical gate length (L_g) of Metal Oxide Semiconductor Field Effect transistor (MOSFET**)** shrinks, the effective channel length (L_{eff}) of the MOSFET device will be decreased. The close proximity between the source region and the drain region will reduce the ability of the gate to control the threshold voltage (V_{TH}) and the flow of the current in the channel [2]. The increase of electrostatic effect in the channel region will eventually lead to short channel effect (SCE) problems. Therefore, conventional MOSFET architecture are not suitable to be scaled down below 20nm technology [3]. In order to suppress SCEs, the gate to channel coupling must be increased with respect to source/drain coupling to channel coupling. This could be realized by having one extra gate in MOSFET device to suppress SCEs and thus doubling the drive current (I_{ON}).

One of the common types of double-gate MOSFET is known as **VDG-MOSFET**. The basic architecture of VDG-MOSFET consists of a silicon pillar of few tenth of nanometer in length, which is regarded as the active area of the MOSFET [4]. The channel length of the Vertical DG-MOSFET is normally adjusted by oblique rotation ion implantation (ORI), diffusion techniques. The advantage of the Vertical DG-MOSFET is that the channel length is not dependent on the use of lithography. It can be easily fabricated with both back gates aligned together [5]. The main advantage of this architecture is due to its high possibility in reducing short channel effect (SCE).

Short channel effect (SCE) has become the major threat in conventional MOSFET device structure. SCE occurs when the source and drain region become too close to each other. If the effective channel length (L_{eff}) becomes too short, the depletion region from drain will reach the source region and subsequently reduces the barrier for electron injection. As consequences, leakage current (I_{OFF}) and drain induced barrier lowering (DIBL) will be increased. The vertical pillar is then be constructed in order to prevent SCE problems. As the drain region is located on the top of pillar, the effective channel length (L_{eff}) will not be dependent with physical gate length (L_g). Hence, any reduction on physical gate length (L_g) does not affect much on the effective channel length (L_{eff}).

The good switch-off characteristic of a Vertical DG-MOSFET can be realized by gate to gate capacitive coupling [6]. The voltage of both sides of the gates swing synchronously and then induces the same amount of potential charge within the channel. This will create an excellent electrostatic control of the gate over the sub-threshold leakage current. It shows how much change in the gate voltage is required to change the drain current by one decade. This

response characteristic is known as sub-threshold swing and is expressed in (1) [2]:

$$SS = \left[\frac{dV_{GS}}{d(\log_{10} I_{DS})} \right] \quad (1)$$

For the purpose of scaling down the dimension of VDG-MOSFET, physical gate length (L_g) and silicon pillar length (L_p) are reduced. However, it has to be done by using an appropriate etching technique. The technique named as ion-bombarded-retarded etching (IBRE) had been introduced in order to form an ultra-thin pillar in VDG-MOSFET device [7]. This unique etching technique utilizes a hot alkaline solution which enables Si substrate being etched anisotropically. Si etch rate (ER) in an alkaline solution is low and thus reduce the possibility of Si damage during ion implantation.

A proper design consideration must be taken in order to virtually fabricate a proper Ultrathin Pillar (UTP) VDG-MOSFET for low power (LP) technology. According to International Technology Roadmap Semiconductor (ITRS) 2013 for year 2014, the threshold voltage (V_{TH}) must be in the range of ±12.7% of ITRS 2013 prediction (0.453V) [8]. In other words, the V_{TH} value has to be within range of 0.395V to 0.511V. Drive current (I_{ON}) is expected to be equal or more than 610µA/µm. Meanwhile, the off-state leakage current (I_{OFF}) must be equal or more than 10ρA/µm [8]. The simplified ITRS 2013 specification table is shown in Table I.

TABLE I. ITRS 2013 SPECIFICATION FOR LOW POWER (LP) TECHNOLOGY REQUIREMENT [8]

Electrical Response	**ITRS 2013 Specification**
Threshold Voltage (V_{TH})	±12.7% of 0.453V
Drive Current (I_{ON})	≥ 610 µA/µm
Leakage Current (I_{OFF})	≥ 10 ρA/µm

II. MATERIAL AND METHODS

A. *UTP VDG-MOSFET Device Design Using SILVACO TCAD*

Three novel designs are introduced which are named as Ultrathin Pillar (UTP) VDG-MOSFET, UTP Silicon-on-insulator (SOI) VDG-MOSFET and UTP Polysilicon-on-insulator (POI) VDG-MOSFET as illustrated correspondingly in Fig. 1a, Fig. 1b and Fig. 1c. These MOSFET's designs utilize the same methodology except for level concentration of certain dopants and the type of used insulator.

Fig. 1a depicted the layout of UTP VDG-MOSFET device which consists of two physical gates with length of 12nm. The Si-pillar is etched until its length reaches 12nm. The drain region is located on the top of vertical Si-pillar to widen the effective channel length (L_{eff}). However, there is a major disadvantage of this design which is high overlap capacitances [5]. High overlap capacitance may cause a great decrease in drive current (I_{ON}), thus reducing the switching speed operation. The way to reduce the effect of overlap capacitance is by developing **SOI** and **POI** formation as illustrated in Fig. 1b and Fig. 1c. The performance of these three models of MOSFET are investigated by comparing their corresponding electrical characteristics.

Fig. 1a depicted the layout of UTP VDG-MOSFET device which consists of two physical gates with length of 12nm. The Si-pillar is etched until its length reaches 12nm. The drain region is located on the top of vertical Si-pillar to widen the effective channel length (L_{eff}).

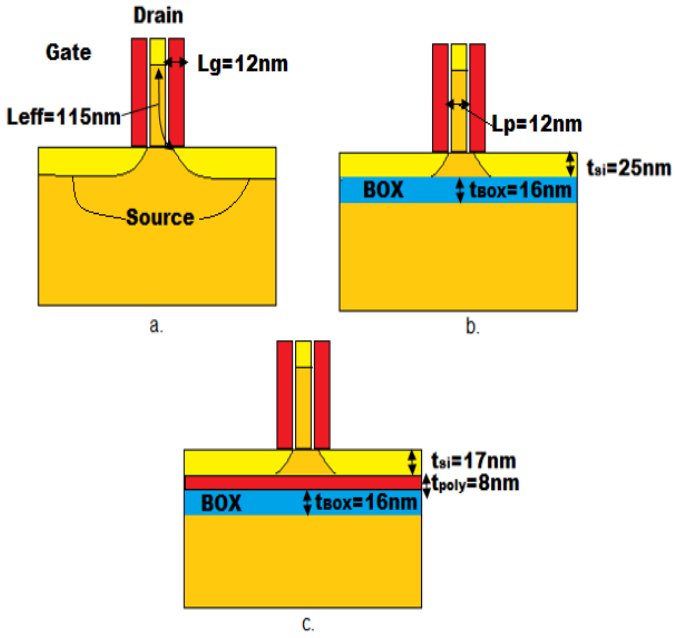

Fig. 1. UTP VDG-MOSFET layout (a) Without SOI (b) SOI (c) POI

Since the UTP POI VDG-MOSFET device is an upgraded model based on the architecture of the previous two models, the methodology of UTP POI VDG-MOSFET device are preferred to be discussed in this section. A UTP POI VDG-MOSFET device was simulated by using **ATHENA** module in SILVACO TCAD tools. Initially, a P-type silicon with <100> orientation was used as the main substrate for this research project. Silicon substrate was then injected by boron with concentration of $1x10^{14}$ atom/cm3. The formation of buried oxide (BOX) was developed by depositing 16nm oxide thickness (t_{BOX}). After that, enhanced channel was created on the top of the BOX by depositing polysilicon material with 8nm of thickness. This formation was known as polysilicon-on-insulator (POI) which was able to suppress SCEs by reducing the amount of charge carriers penetrating the depletion region. The mobility of charge carriers in the channel region becoming more rapid, hence increasing the drive current (I_{ON}).

The silicon was then etched in order to form a very thin pillar which separates the two gates. The virtual process was followed by the gate oxidation process at temperature of 930

C^o. The gate oxidation process used the dry oxidation method instead of wet oxidation because the thickness of oxidation can be better controlled through dry oxidation. The thickness of gate oxide was a very important parameter in vertical dimension that determines the gate control. The next step was to dope a substrate ion (boron) into the silicon substrate with concentration of $9.81x10^{12}$ atom/cm^3 at energy level of 20kev with tilt angle of 7. This was done for the purpose of threshold voltage adjustment in the UTP POI VDG-MOSFET device.

The next simulation process was to deposit polysilicon on top of the gate oxide. The polysilicon was etched away to form a polysilicon gate with length of 12nm. The polysilicon gate was then oxidized at temperature of 870 C^o. The gate was made of polysilicon due to its ability of preventing source/drain ions to be penetrated into a channel region. Phosphor dosage of $3.63x10^{14}$ atom/cm3 was then doped into polysilicon gate along with energy level of 20 kev at tilt angle of 10. This was done in order to increase the conductivity since polysilicon is a low conductivity metal. The conductivity of the gate would affect the switching frequency of the MOSFET device.

In order to achieve an optimum performance for UTP POI VDG-MOSFET device, indium with dosage of $2.61x10^{13}$ atom/cm^3 was doped at energy of 170 kev and tilt angle of 24 into the substrate. Halo implantation was followed by depositing sidewall spacers. Sidewall spacers were then used as a mask for source/drain implantation. Arsenic atom with concentration of 1.22×10^{18} atom/cm^3 at energy level of 43 kev and tilt angle of 80 was implanted to ensure the smooth current flow in UTP POI VDG-MOSFET device. Compensation implantation is utilized later by implanting phosphor dosage of 2.51×10^{12} atom/cm3 at energy level of 60 Kev and tilt angle of 7. This step is taken in order to reduce parasitic effects that could lowering the drive current (I_{ON}).

Next, silicide (CoSi) was formed on the source and drain region by sputtering cobalt on silicon surface. This transistor was then connected with aluminum metal. The aluminum layer was deposited on the top of the Intel-Metal Dielectric (IMD) and unwanted aluminum was etched to develop the contacts [9]-[10]. The procedure was completed after the metallization and etching were performed for the electrode formation, and the bonding pads were opened. The final UTP POI VDG-MOSFET device structure was completed by mirroring the right-hand side structure. The final structure of UTP POI VDG-MOSFET device is illustrated as in Fig 2. The overall flowchart of virtual fabrication process of UTP POI VDG-MOSFET device is shown in Fig. 3.

After the devices were built by utilizing ATHENA module, the designed device was then simulated in **ATLAS** module in order to extract electrical characteristics such as the I_D versus V_{GS} curve. The value of threshold voltage (V_{TH}), drive current (I_{ON}), leakage current (I_{OFF}) and subs-threshold swing (SS) values was then extracted from that particular curve.

Almost the same methodology are utilized in designing both UTP VDG-MOSFET device and UTP SOI VDG-MOSFET device. The differences are at the level of doping concentration and the type of material used as insulator. The final structure of UTP VDG-MOSFET device and UTP SOI VDG-MOSFET device are depicted correspondingly in Fig. 4 and Fig. 5.

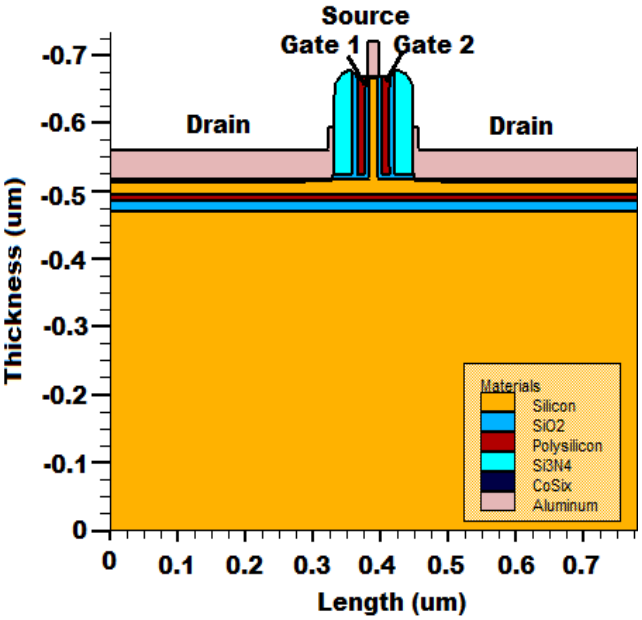

Fig. 2. Final Structure of UTP POI VDG-MOSFET device

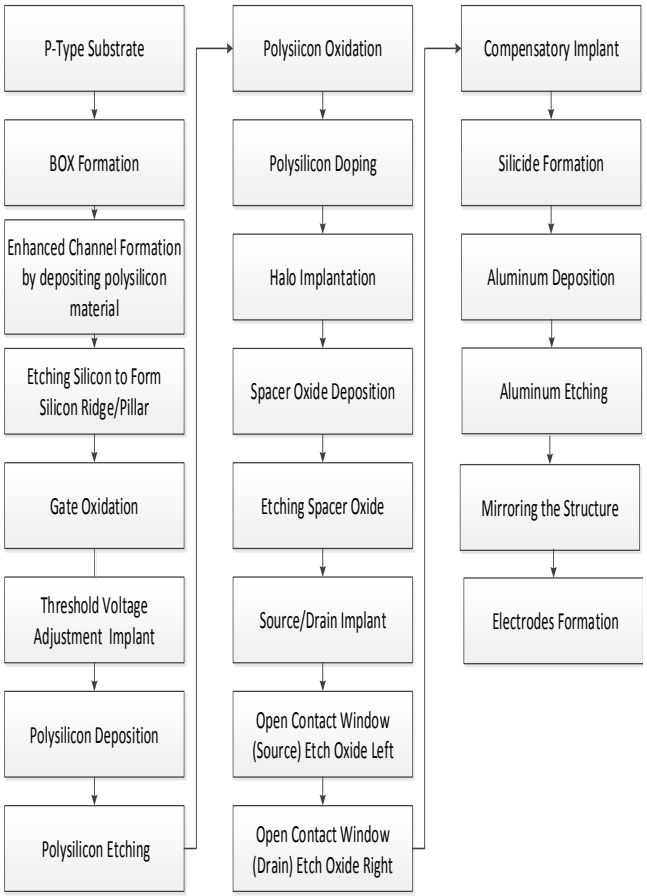

Fig. 3. UTP POI VDG-MOSFET Process Flowchart

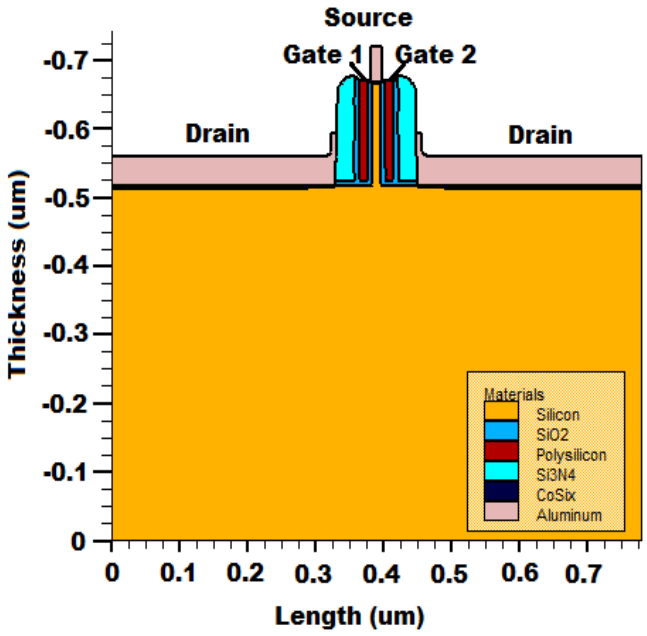

Fig. 4. Final Structure of UTP VDG-MOSFET device

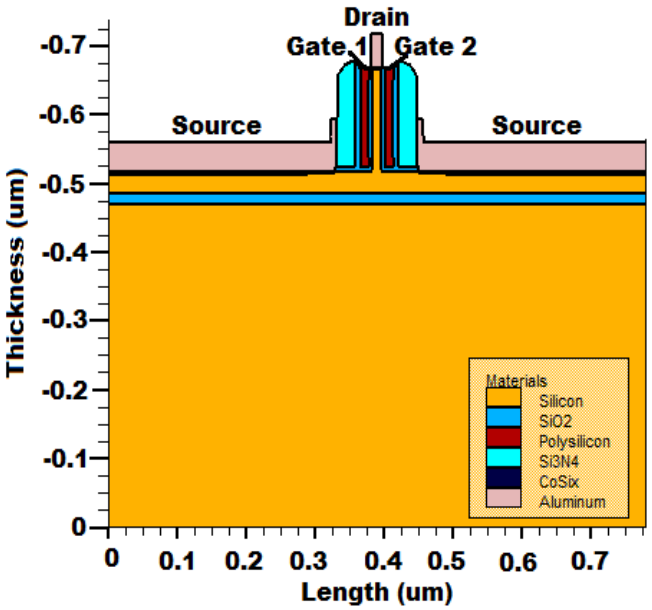

Fig. 5. Final Structure of UTP SOI VDG-MOSFET device

B. Device Characterization

Electrical characteristics for all types of UTP VDG-MOSFET device were experimented by comparing the value of their corresponding threshold voltage (V_{TH}), drive current (I_{ON}), off-leakage current (I_{OFF}), I_{ON}/I_{OFF} ratio and sub-threshold swing (SS). All retrieved values for each individual type of UTP VDG-MOSFET device were compared among each other for comparison analysis. Characterization analysis that have been presented in this study were obtained by utilizing SILVACO TCAD software, ATLAS module.

It is essential to ensure that all types of UTP VDG-MOSFET device are producing a quite similar value of threshold voltage (V_{TH}) among each other in order to precisely evaluate their performance. The value of threshold voltage (V_{TH}) must be within ±12.7% of ITRS 2013 prediction. The input process parameters that have been used in the design of UTP VDG-MOSFET device were substrate implant dose, halo implant tilt angle, gate-oxide diffusion temperature, threshold voltage (V_{TH}) implantation dose, V_{TH} implantation energy, halo implantation dose, halo implantation energy, source/drain (S/D) implantation dose, S/D implantation energy, compensatory implantation dose, compensatory implantation energy and etc. The detail amount of input process parameters used in all the MOSFET designs were summarized in Table II.

The initial point for the characterization simulation is a structure represented in Fig. 2. Fig. 4 and Fig. 5. The SOI and POI structures are believed to have higher immunity to SCEs compared to the reference design. It is mainly because of the BOX formation is able to trap most of the charge carriers in the channel. This will subsequently increases the mobility of ions in the channel region, hence boosting the drive current (I_{ON}). The presence of polysilicon on the top of BOX formation is

believed to enhance the channel capacity, thus increasing the mobility of charge carriers.

TABLE II. INPUT PROCESS PARAMETERS OF UTP VDG-MOSFET DEVICE

Process Parameters		**UTP VDG-MOSFET device**	**UTP SOI VDG-MOSFET device**	**UTP POI VDG-MOSFET device**
	Units	***Level***		
Substrate Implantation Dose	atom cm^{-3}	1e14	1e14	1e14
V_{TH} Implantation Dose	atom cm^{-3}	1.81e12	1.81e12	9.81e12
V_{TH} Implantation Energy	kev	20	20	20
V_{TH} Implantation Tilt	degree	7	7	7
Halo Implantation Dose	atom cm^{-3}	1.33e13	2.04e13	2.61e13
Halo Implantation Energy	kev	170	170	170
Halo Implantation Tilt	degree	24	24	24
S/D Implantation Dose	atom cm^{-3}	1.25e18	1.25e18	1.22e18
S/D Implantation Energy	kev	45	45	43
S/D Implantation Tilt	degree	80	80	80
Compensatory Implant Dose	atom cm^{-3}	2.51e12	2.51e12	2.51e12
Compensatory Implant Energy	kev	62	62	60
Compensatory Implant Tilt	degree	7	7	7

III. RESULTS AND DISCUSSION

The electrical characteristic results for all three types of UTP VDG-MOSFET device were obtained by utilizing ATLAS module. Later, the final results of electrical response for all UTP VDG-MOSFET devices were compared among each other. The electrical performance for each individual device were the compared and analyzed.

A. Analysis of Vertical DG-MOSFET Device

Fig. 6 shows the doping concentration across the UTP VDG-MOSFET device. The figure indicates the doping concentration of silicon, silicon dioxide, polysilicon, silicon nitride and aluminum. Doping concentration is regarded as one of the important factors in the fabrication process. An accurate doping concentration will ensure the UTP VDG-MOSFET device are working well with an excellent gate control, high drive current (I_{ON}), very low leakage current (I_{OFF}), ideal sub-threshold swing (SS) and high I_{ON}/I_{OFF} ratio.

Fig. 7 depicts the graph of drain current (I_D) versus gate voltage (V_G) at drain voltage (V_D) = 1.0V for all types of UTP VDG-MOSFET device. The expected nominal value of threshold voltage (V_{TH}) specified in ITRS 2013 for year 2014 is 0.453V. The threshold voltage (V_{TH}) values extracted from the graph for UTP VDG-MOSFET device, UTP SOI VDG-MOSFET device and UTP POI VDG-MOSFET device were observed to be 0.417V, 0.419V and 0.419V respectively. All the values were acceptable since their value's range was still within ±12.8% of ITRS 2013 prediction (0.453V) [8].

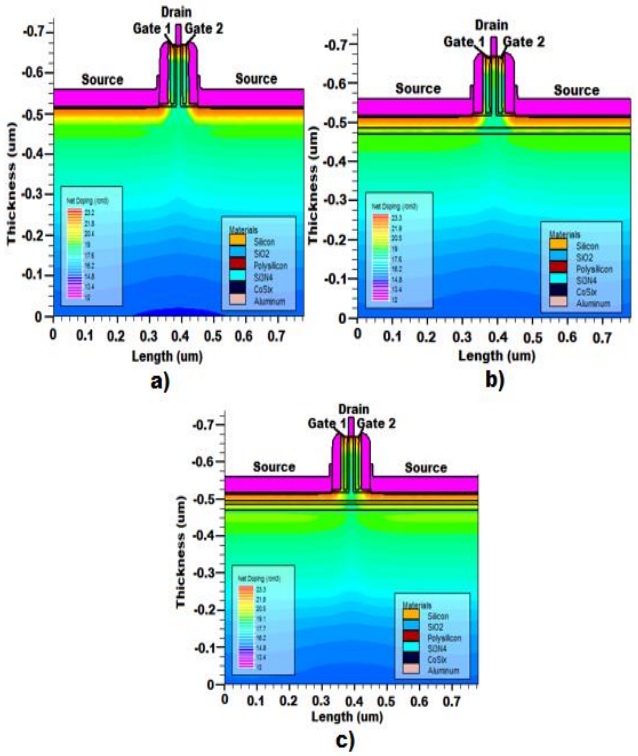

Fig. 6. Contour Mode of UTP VDG-MOSFET layout (a) Without SOI (b) With SOI (c) With POI

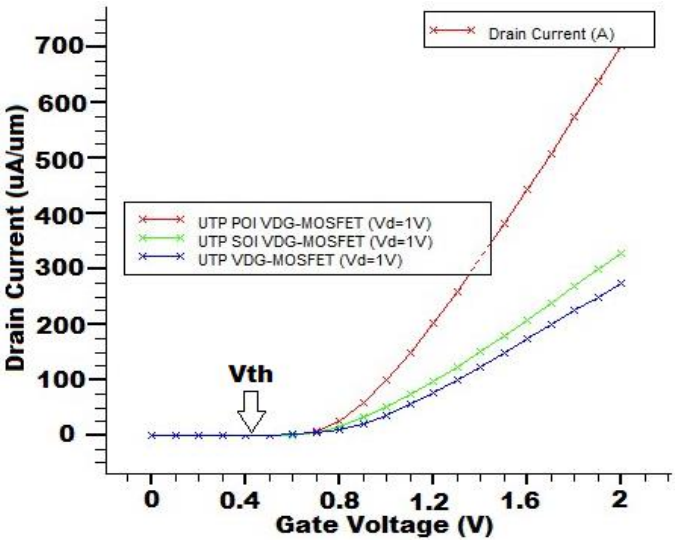

Fig. 7. Graph I_D-V_G for UTP VDG-MOSFET devices

Fig. 7 shows the graph of sub-threshold drain current (I_d) versus gate voltage (V_G) at drain voltage (V_D) = 1.0 V for UTP

VDG-MOSFET device, UTP SOI VDG-MOSFET device and UTP POI VDG-MOSFET device. The value of the off-leakage current (I_{OFF}) and drive current (I_{ON}) for each individual MOSFET can be extracted from the graph.

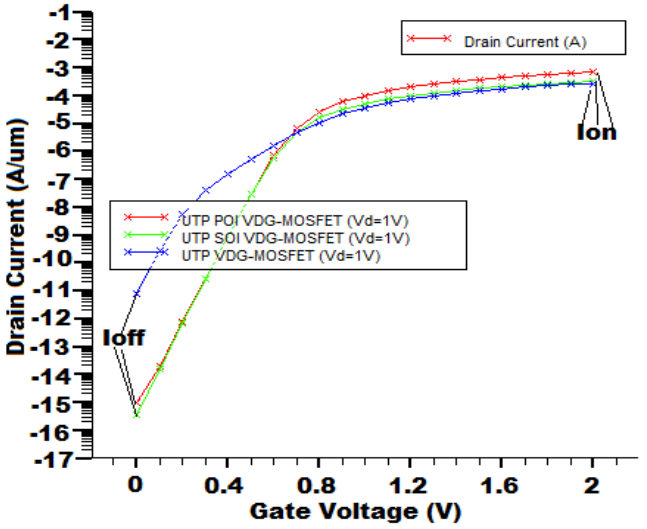

Fig. 8. Graph Sub-threshold I_D-V_G for UTP VDG-MOSFET devices

Based on the results extracted from the graph in Fig. 8, it was observed that the values of drive current (I_{ON}) for UTP VDG-MOSFET device, UTP SOI VDG-MOSFET device and UTP POI VDG-MOSFET device were 274.3 µA/µm, 329.6 µA/µm and 704.6 µA/µm respectively. Meanwhile, the values of leakage current (I_{OFF}) for UTP VDG-MOSFET device, UTP SOI VDG-MOSFET device and UTP POI VDG-MOSFET device were found to be 8.293e-12 µA/µm , 3.567e-16 µA/µm and 9.775e-16 µA/µm respectively.

B. Performance Comparison among UTP VDG-MOSFET Devices

For the purpose of investigating the electrical performance of UTP VDG-MOSFET devices, several electrical responses of each individual type of MOSFETs were recorded to be compared and analyzed. The detail performance comparison among all types of UTP VDG-MOSFET device are summarized in Table III.

TABLE III. PERFORMANCE COMPARISON OF UTP VDG-MOSFET DEVICES

Electrical Responses	**UTP VDG-MOSFET Device**	**UTP SOI VDG-MOSFET Device**	**UTP POI VDG-MOSFET Device**	**Expected Range of Value**
V_{TH} (V)	0.417	0.419	0.419	±12.7% of 0.453
I_{ON} (µA/µm)	274.3	329.6	704.6	≥ 610
I_{OFF} (A/µm)	8.293e-12	3.567e-16	9.775e-16	≥ 10ρ
I_{ON}/I_{OFF} Ratio	33.08e6	9.24e11	7.208e11	≥ 10^6
SS (mV/dec)	65.06	60.72	63.52	60-65

The threshold voltage (V_{TH}) of all types of UTP VDG-MOSFET device are set to be a reference value and its value is set to be as close as possible towards each other. This is done in order to ensure other electrical characteristics are precisely computed by ATLAS module of SILVACO TCAD tools. From Table III, it can be observed that all the threshold voltage (V_{TH}) for each types of UTP VDG-MOSFET device are within the range of 0.417V-0.419V. Since these results are still in the range of ±12.7% of 0.453V (ITRS 2013) [8], they are acceptable to be selected as reference values for each corresponding designs.

The second electrical response is known as drive current (I_{ON}). From Table III, it is observed that only drive current (I_{ON}) of UTP POI VDG-MOSFET device (704.6 µA/µm) exceeds the expected requirement which is 610 µA/µm. Meanwhile, drive current (I_{ON}) for both UTP VDG-MOSFET device and UTP SOI VDG-MOSFET device are observed to be 274.3 µA/µm and 329.6 µA/µm. Both of these results are far from the expected value, thus they are not applicable for low power (LP) technology. A high drive current (I_{ON}) value indicates an excellent driving capability of MOSFET device.

For leakage current (I_{OFF}), all types of UTP VDG-MOSFET device possess a value that exceeds 10 ρA/µm. Based on Table III, UTP SOI VDG-MOSFET device produces the lowest leakage current (I_{OFF}) at 3.567e-16 A/µm. For both UTP VDG-MOSFET device and UTP POI VDG-MOSFET device, the leakage current (I_{OFF}) values are 8.293e-12 A/µm and 9.775e-16 A/µm respectively. A low leakage current (I_{OFF}) indicates excellent suppression of short channel effect (SCE).

In order to determine the power consumption of each individual UTP VDG-MOSFET device, the I_{ON}/I_{OFF} ratio are computed and analyzed. Based on the computation results in Table III, all types of UTP VDG-MOSFET device produce I_{ON}/I_{OFF} ratio above 10^6. The higher I_{ON}/I_{OFF} ratio is, the lower power consumption will be. Therefore, it can be observed that I_{ON}/I_{OFF} ratio of UTP SOI VDG-MOSFET device is the highest value which is 9.24e11. Meanwhile, the I_{ON}/I_{OFF} ratio for both UTP VDG-MOSFET device and UTP POI VDG-MOSFET device are 33.08e6 and 7.208e11. There are slightly decrease on I_{ON}/I_{OFF} ratio value for UTP POI VDG-MOSFET device compared to UTP SOI VDG-MOSFET device. This shows that UTP SOI VDG-MOSFET device has slightly lower power consumption than UTP POI VDG-MOSFET device.

The final response which has been investigated is called sub-threshold swing (SS). Sub-threshold swing (SS) is an important electrical response in UTP VDG-MOSFET device which is able determine how fast the switching operation from "OFF" state to "ON" state or vice versa. The lower SS value is, the faster the switching operation will be. The ideal SS value for MOSFET device is in the range of (60-65) mV/dec. Based on the results in Table III, it is observed that UTP SOI VDG-MOSFET device produce the lowest SS value at 60.72mV/dec. Meanwhile, SS values for both UTP VDG-MOSFET device and UTP POI VDG-MOSFET device are 65.06 mV/dec and 63.52 mV/dec correspondingly. The values are still within the predicted range.

From the overall performance observation, only UTP POI VDG-MOSFET device satisfies all the expected value's range of electrical responses. The UTP SOI VDG-MOSFET device seems to be better in almost electrical responses but its drive current (I_{ON}) value are lower than 610 µA/µm [8]. Therefore, UTP POI VDG-MOSFET device is recognized as the ideal design consideration for low power (LP) technology in ITRS 2013.

IV. CONCLUSION

In conclusion, three designs of MOSFET named as UTP VDG-MOSFET device, UTP SOI VDG-MOSFET device and UTP POI VDG-MOSFET device are succesfully designed by utilizing SILVACO TCAD, ATHENA and ATLAS modules. The UTP POI VDG-MOSFET device has been recognized as the most ideal design for low power (LP) application due to its excellent electrical characteristics. The electrical characteristics of UTP POI VDG-MOSFET device is observed to meet the low power (LP) technology requirement of ITRS 2013 for year 2014. The drive current (I_{ON}) of UTP POI VDG-MOSFET device exceeds the minimum value of 610 µA/µm as specified in ITRS 2013. The presence of both BOX and enchanced polysilicon channel formation are able to prevent excessive charge sharing within the source region. Both of these formation are capable of increasing the depeletion region under the gate, thus trapping more charge carriers in the source region. The rapid mobility of ion movement in the channel tremendously increases the drive current (I_{ON}). Futhermore, the leakage current (I_{OFF}) of UTP POI VDG-MOSFET device is observed to be very low due to the BOX's abilty in reducing the encroachment of the drain's electric field. A very low leakage current (I_{OFF}) indicates an excellent suppression of short channel effects (SCEs). Based on the retrieved results, the threshold voltage (V_{TH}) and drive current (I_{ON}) values of UTP POI VDG-MOSFET device are observed to be 0.419 V and 704.6 µA/µm respectively.

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